



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MIC/14/8389
Dated 07 May 2014

**Pure Tin Lead finishing products - Transfer assembly &
test sites from Amkor ATK (Korea) to Amkor ATP (Philippines)**

Table 1. Change Implementation Schedule

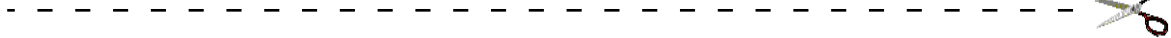
Forecasted implementation date for change	07-Nov-2014
Forecasted availability date of samples for customer	03-Oct-2014
Forecasted date for STMicroelectronics change Qualification Plan results availability	03-Oct-2014
Estimated date of changed product first shipment	07-Nov-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	STM32F100VCT6, pure Tin Lead finishing products
Type of change	Package assembly location change
Reason for change	Amkor ATK1 (Korea) assembly site closure
Description of the change	Due to Amkor ATK1 (Korea) assembly site closure, ST Microcontrollers Division intends to transfer manufacturing sites from Amkor ATK (Korea) to Amkor ATP (Philippines).
Change Product Identification	See indicated below
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN MMS-MIC/14/8389
Please sign and return to STMicroelectronics Sales Office		Dated 07 May 2014
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name: Title: Company: Date: Signature:	
Remark		

DOCUMENT APPROVAL

Name	Function
Colonna, Daniel	Marketing Manager
Buffa, Michel	Product Manager
Narche, Pascal	Q.A. Manager



PRODUCT/PROCESS CHANGE NOTIFICATION

Pure Tin Lead finishing products - Transfer assembly & test sites from Amkor ATK (Korea) to Amkor ATP (Philippines)

MMS - Microcontrollers Division (MCD)

Dear Customer,

Due to Amkor ATK1 (Korea) assembly site closure, ST Microcontrollers Division intends to transfer manufacturing sites from Amkor ATK (Korea) to Amkor ATP (Philippines).

What are the changes?

For Pure Tin Lead finishing products:

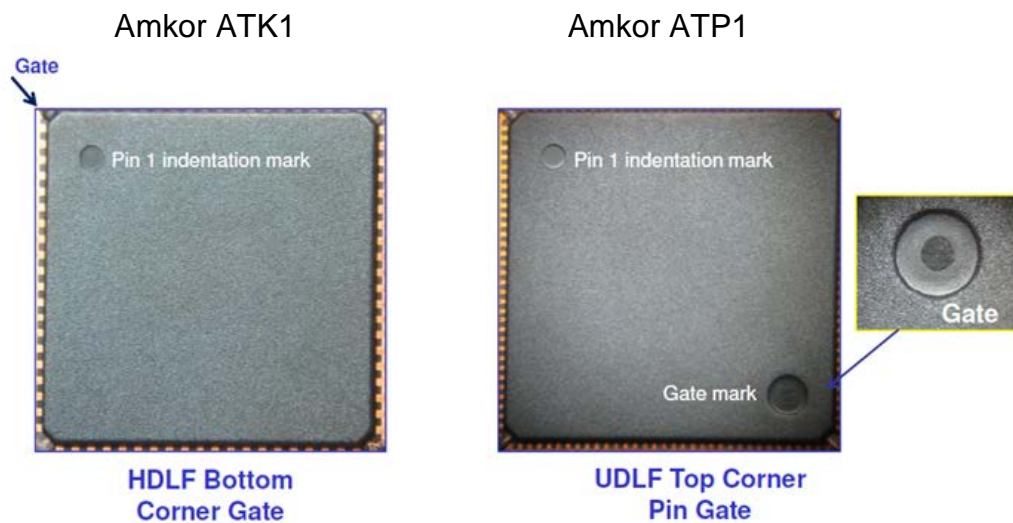
New Bill Of Material is described below:

	Previous	New
Assembly site	Amkor ATK1 (Korea)	Amkor ATP1 (Philippines)
Test site	Amkor ATK3 (Korea)	Amkor ATP3 (Philippines)
Mold compound	Sumitomo G700L	Sumitomo G631HQ
Glue	Ablestik 3230	Evertech AP4200
Leadframe	High Density Lead Frame (HDLF)	Ultra high Density Lead Frame (UDLF)

Chosen Bill Of Material is standard Bill Of Material, already running in high volumes for LQFP at Amkor ATP (Philippines).

Gate mark on Ultra high Density Lead Frame:

An additional gate mark is visible on top of the package, in addition to pin 1 identification mark.



Why ?

Due to Amkor ATK1 (Korea) assembly site closure, ST MCD division moves production from Amkor ATK (Korea) to Amkor ATP (Philippines).

When ?

The production on the new platform will start week 45 2014.

How will the change be qualified?

This change will be qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard. You can find below Qualification Plan.

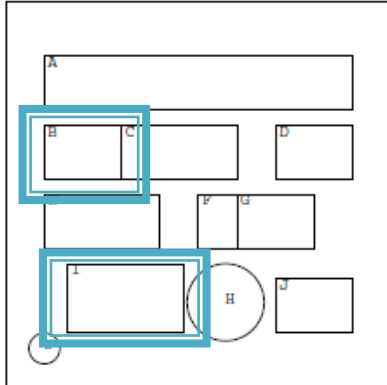
What is the impact of the change?

- **Form:** Gate mark added
- **Fit:** no change
- **Function:** no change

How can the change be seen?

Traceability of the change is ensured by ST internal tools.

The marking instruction indicated on the products is changing from:



B : Assembly plant change from HP to 7B

I : Country Of Origin change from KOR to PHL

We remain available to discuss any concern that you may have regarding this Product Change Notification.

With our sincere regards.

Michel Buffa

Microcontroller Division General Manager



RERMCD 1312- Pure Sn QUALIFICATION PLAN

Qualification of :

LQFP14x14 & 20X20 at Amkor Philippines for Microcontrollers devices

Qualification Reference :	RERMCD1312
Issued on :	Mar 31, 2014
Assembly Plant :	AMKOR Philippines (ATP)
Assembly Line :	LQFP
Package / Process :	14x14- 100Leads
Device :	STM32
Lead termination:	PURE SN
MSL:	MSL3

**Purpose**

Qualification of new assembly lines for Microcontrollers in LQFP packages assembled at ATP (Philippines) .

Ultra High Density Lead Frame will be qualified: an additional gate mark is visible on top of the package, in addition to pin 1 identification.

Test Vehicles :

Package line	Assembly Line	Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
1	LQFP14*14	100L	STM32F (1L*414)	TSMC	1

Assembly line qualification will be done upon PPF qualification plan reference MCDRER1312-PPF.

Package Reliability Trials :

(*) tests performed after preconditioning

Reliability Trial	Test Conditions	Pass Criteria	Unit per Lot	Qual Lot nb	
PC	Pre Conditioning: Moisture Sensitivity Jedec Level 3 J-STD-020/ JESD22-A113	Bake (125°C / 24 hrs) Soak (30°C / 60% RH / 192 hrs) for level 3 Convection reflow: 3 passes with Jedec level 3	3 passes MSL3	308	1
AC or Uhast(*)	Autoclave JESD22 A102 UnBiased Highly Accelerated Temperature and Humidity Stress JESD22 A118	121°C, 100% RH, 2 Atm 130°C, 85%RH, 2 atm	96h	77	1
TC(*)	Thermal Cycling JESD22 A104	-50°C, +150°C	1000Cy	77	1
THB(*)	Temperature Humidity Bias JESD22 A101	85°C, 85% RH, bias	1000h	77	1



THS(*)	Temperature Humidity Storage JESD22 A110	85°C, 85% RH, no bias	1000h	77	1
HTSL	High Temperature Storage Life JESD22 A103	150°C- no bias	1000h	77	1
ESD	ESD Charge Device Model ANSI/ESDSTM5.3.1	750V corners 500V all other pins	750V / 500V	3	1
Physical dimension	Dimension measurement JESD 22B100/B108		CPK >1.33 PPK >1.67	10	1
Solderability	Lead solderability JESD 22B102		>95% lead coverage	45 leads	1

Attachment : Reliability tests description

Package oriented tests/ Trials description

1. Preconditioning

According to ST spec 0098044.

Preconditioning test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good modeling of the life of the packaged product.

Out-of-bag floor life storage and soldering are modeled by the following test sequence:

- Bake to completely remove moisture from the package;
- Moisture soak according to the package moisture level;
- IR reflow.

The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder reflow process. This phenomenon can create plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.

2. Autoclave (AC)

The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.

Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

To point out critical water entry paths with consequent electrochemical and galvanic corrosion.



1. Unbiased Highly Accelerated Temperature and Humidity Stress (UHASt)

The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.

2. Temperature Cycling (TC)

The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).

Purpose: to investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system.

Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.

3. Temperature Humidity Bias (THB)

The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.

The Temperature Humidity Bias follows the same method than HAST at lower temperature.

Purpose: to investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions.

Typical failure mechanisms are electro-chemical corrosion and surface effects related to the molding compound.

The package moisture resistance with electrical field applied is verified, both electrolytic and galvanic corrosion are put in evidence.

Conditions:

- $T_a=85^{\circ}\text{C}$; R.H.=85%;
- Power supply voltage less or equal to max operative voltage to not exceed $T_j = 95^{\circ}\text{C}$.

4. Temperature Humidity Storage (THS)

The Temperature Humidity Storage is stored at controlled conditions of high temperature and relative humidity.

The Temperature Humidity Storage follows the same method than Unbiased HAST at lower temperature.

Purpose: to evaluate the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package.

- Test conditions: 85°C / 85% RH.
- No power supply

5. High Temperature Storage Life (HTSL)

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.

Purpose: to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.

1. ESD Charge Device Model (CDM)

This ESD failure model is associated with the device and package itself. The CDM is intended to simulate charging/discharging events that occur in production equipment and processes. The Field induced CDM equivalent circuit used to describe this phenomenon is illustrated in Figure 1.

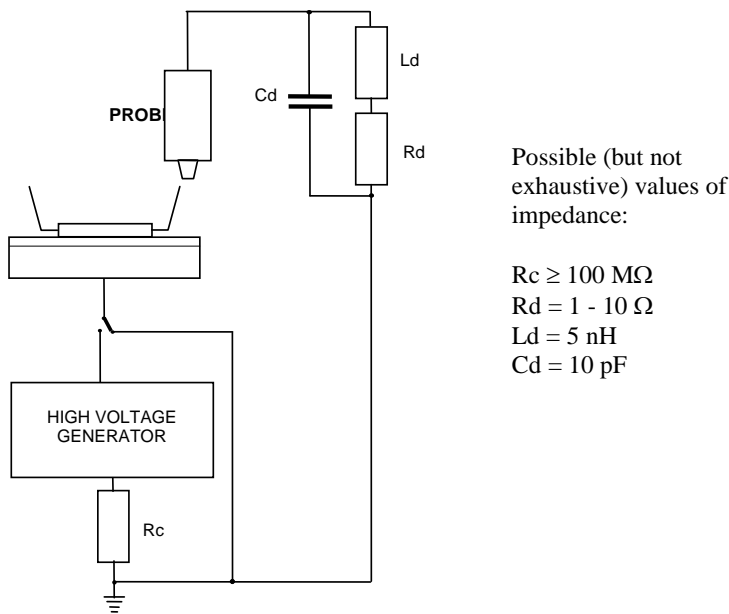


Fig.1 : Field induced CDM equivalent circuit

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